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My name and post office address are as stated below;

That I am knowledgeable in the English language and in the Japanese language and that I believe the English translation of the Japanese patent application No. **10-291995** is a true and complete translation of the above identified patent application as filed.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: October 28, 2005

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[Document name] SPECIFICATION

[Title of the invention] Digital Camera

[Claims]

[Claim 1]

A digital camera, comprising:

a CCD imager having a first resolution;

an output means for outputting a first resolution image signal from said CCD imager;

a thinning-out means for performing a thinning-out process on said first resolution image signal to generate a second resolution image signal with a resolution lower than said first resolution image signal;

a main memory having at least two memory areas;

a designating means for selectively designating each of said two memory areas;

a main writing means for writing said second resolution image signal in one of said two memory areas on the basis of the output from said designating means; and

a main reading means for reading said second resolution image signal from the other of said two memory areas on the basis of the output from said designating means.

[Claim 2]

A digital camera according to claim 1, wherein

said output means outputs one screen of said first resolution image signal for every first predetermined time period, and

said main reading means reads one screen of said second resolution image signal for every second predetermined time period with shorter in length than said first predetermined time period.

[Claim 3]

A digital camera according to claim 2, wherein said designating means alternately switches the memory area to be designated for every first predetermined time period.

[Claim 4]

A digital camera according to any one of claims 1 to 3, wherein

a shutter button;

a first disabling means for disabling said thinning-out means in response to an operation of said shutter button;

a second disabling means for disabling said main reading means in response to the operation of said shutter button; and

a third disabling means for disabling said main writing means when said one screen of said first resolution image signal is written to said main memory.

[Claim 5]

A digital camera according to claim 4, comprising:

a first request signal output means for outputting a first request signal to request writing of said second resolution image signal to said main memory, and

a second request signal output means for outputting a second request signal to request reading of said second resolution image signal from said main memory, wherein

said second disabling means includes a second request gating means for applying gating to said second request signal; and

said third disable means includes a first request gating means for applying gating to said first request signal.

[Claim 6]

A digital camera according to any one of claims 1 to 5 further comprising a monitor for displaying an image corresponding to said second resolution image signal.

[Detailed description of the invention]

[0001]

[Field of the invention]

The present invention relates to digital cameras and, more particularly, to a digital camera for displaying subject motion images (through images) shot in real time on the monitor.

[0002]

[Prior art]

Where displaying subject through-images having been shot by a digital camera on a built-in monitor, the display image if utilizing an NTSC format requires to be renewed every 1/30 second. Due to this, the shot image data on each frame has to be processed within a brief time, in order to be in time for renewal timing. Meanwhile, the increase in the number of pixels for the CCD imager, in turns, increases the data amount of each frame. Accordingly, process failure might result unless an improvement is contemplated for the processing method.

[0003]

For this reason, in the conventional digital cameras having pixels in number exceeding one million for example, the pixels to be read out of the CCD imager are subjected to thinning out prior to being outputted for through-images. That is, this includes a process that all the pixels are read out upon depressing the shutter button. However, when outputting a through-image, pixel thinning-out is implemented in order to decrease the amount of data.

[0004]

[Problem to be solved by the invention]

However, the conventional method includes switching the pixel read-out scheme between upon outputting through-images and at pressing on the shutter. Consequently,

there has been a problem that the CCD imager is complicated in control and hence the circuit therefor becomes complex in configuration.

It is therefore an object of the present invention to provide a novel digital camera which is capable of preventing against process failure.

[0005]

[Means to solve the problem]

The present invention is a digital camera comprising a CCD imager having a first resolution, an output means for outputting a first resolution image signal from the CCD imager, a thinning-out means for performing a thinning-out process on the first resolution image signal to generate a second resolution image signal with a resolution lower than the first resolution image signal, a main memory having at least two memory areas, a designating means for selectively designating each of the two memory areas, a main writing means for writing the second resolution image signal in one of the two memory areas on the basis of the output from the designating means, and a main reading means for reading the second resolution image signal from the other of the two memory areas on the basis of the output from the designating means.

[0006]

[Operation]

The output means outputs a first resolution image signal from the CCD imager. The outputted first resolution image signal is subjected to a thinning-out process by the thinning-out means, so that a second resolution image signal with a resolution lower than the first resolution image signal is generated. On the other hand, the designating means selectively designates each of the two memory areas belonging to the main memory. The main writing means writes the second resolution image signal in one of the memory areas on the basis of the output from the designating means. The main reading means reads the

second resolution image signal from the other of the memory area on the basis of the output from the designating means.

[0007]

In one aspect of the present invention, the output means outputs one screen of the first resolution image signal for every first predetermined time period, and the main reading means reads one screen of the second resolution image signal for every second predetermined time period with a length shorter than the first predetermined time period. Also, the designating means alternately switches the memory area to be designated for every first predetermined time period.

In another aspect of the present invention, in response to an operation of a shutter button, a first disabling means disables the thinning-out means. Therefore, the second resolution image signal is outputted from the memory buffer in place of the second resolution image signal. When one screen of the first resolution image signal is outputted from the buffer memory, a second disabling means disables the buffer reading means. Additionally, in response to an operation of the shutter button, a third disabling means disables the main reading means.

[0008]

In the other aspect of the present invention, the image corresponding to the second resolution image signal is displayed on the monitor.

[0009]

[Advantage of the invention]

According to this invention, because the first resolution image signal is thinned out and created into a second resolution image signal with a low resolution, no failure will be encountered in signal processing even where the CCD imager has an increased resolution. Meanwhile, while writing is being made to one memory area, reading is

effected from the other memory area. Accordingly, even where there is difference in operation speed between the areas, the operation on one area will not outpace the operation on the other area. Thus, outputted images are free from disturbance.

[0010]

The above described objects and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings

[0011]

[Embodiment of the invention]

Referring to Figure 1, a digital camera 10 of this embodiment includes a CCD imager 12. The CCD imager 12 has a not-shown color filter mounted at a front thereof. An optical image of a subject is given to the CCD imager 12 through the color filter.

[0012]

If an operator operates a mode set switch 56 to a side of camera, a system controller 52 sets for a camera mode. At this time, the CPU 68 starts a signal generator (SG) 16 so that the signal generator (SG) 15 can output a horizontal synchronizing signal and a vertical synchronizing signal. Based on the outputted horizontal and vertical synchronizing signals, a TG 14 creates a timing signal to drive the CCD imager 12 by a progressive scan scheme. The CCD imager 12 has vertical lines in number of "1024" and horizontal pixels in number of "768", so that a camera signal (high resolution camera signal) can be outputted with a resolution of XGA. Incidentally, it takes 1/15 second to output a camera signal for each frame.

[0013]

The outputted camera signal from the CCD imager 12 is a signal that each pixel has any one of color components. The camera signal thus configured is subjected to

well-known noise removal and level adjustment by a CDS/AGC circuit 14, and then converted into camera data as a digital signal by an A/D converter 16. A signal processing circuit 18 performs YUV conversion with a ratio of 4:2:2 on the camera data outputted from the A/D converter 16, thus creating YUV data (high resolution YUV data).

[0014]

To display real-time motion images (through images) of a subject on a monitor 44, a switch SW1 is connected to a side of a thinning-out circuit 24. That is, the thinning-out circuit 24 is enabled during outputting through-images. The outputted high-resolution YUV data from the A/D converter 16 is thinned out by the thinning-out circuit 24, thereby converted into YUV data (low resolution YUV data) having vertical lines in number of "768" and horizontal pixels in number of "480". It should be noted that the pixel data constituting the low resolution YUV data is intermittently outputted without putting close together the pixel data correspondingly to thinning-out.

[0015]

The low resolution YUV data outputted from the thinning-out circuit 24 is sent to a buffer 26a via the switch SW1. The buffer 28 is configured by a dual port SRAM having a capacity corresponding to 128-pixels YUV data. The low resolution YUV data is consecutively written onto the buffer 26a by a buffer write circuit 22a provided in the signal processing circuit 22. That is, the pixel data is put close together in order to eliminate missing portions incurred due to thinning out. This process provides the pixels with an equivalent pitch to that of pixels of before the thinning-out operation.

[0016]

The YUV data written on the buffer 26a is read out by a memory control circuit 30 before overwritten by the succeeding YUV data. The memory control circuit 30 fetches

the read YUV data through a bus 28, and thereafter writes it to an SDRAM 38 through a bus 6. The clock rate to read data from the buffer 26a is set 4 times a clock rate to write data to the buffer 26a. The buses 28 and 36 are occupied to transfer YUV data from the buffer 26a to the SDRAM 38 in a duration of a quarter of the total period.

[0017]

Explanation will be concretely made on write operation to the SDRAM 38 with reference to Figure 2. A read request generating circuit 22b included in the signal processing circuit 22 generates a read request at predetermined timing. A write request generating circuit 42b included in an NTSC encoder 42 also generates a write request at predetermined timing. During outputting through-images, the CPU 68 sends a high level gate signal to AND circuits 22c and 42c. This opens the gate to thereby input read and write requests to a mediation circuit 30a. The mediation circuit 30a mediates between the requests, and outputs a predetermined start signal to the processing circuit 30b in order to respond to any of the requests.

[0018]

To process for a read request from the signal processing circuit 22b, the buffer control circuit 32a sends an address signal to the buffer 26a in response to the start signal and reads YUV data out of the buffer 26a. The read YUV data is fetched into the processing circuit 32b via a bus 28. An SDRAM write circuit 34a writes the fetched YUV data onto the SDRAM 38 through the bus 36. Because the occupation over the buses 28 and 36 at all times excludes other of processing, the processing circuit 30b outputs an end signal to the mediation circuit 30a each time 64-pixels YUV data has been written, thereby opening over buses 28 and 36. Then the mediation circuit 32a enters a next requests process. In this manner, the read requests sent from signal processing circuit 18 are processed in a plurality of number of times, thereby writing 1-frame low

resolution YUV data onto the SDRAM 38 in 1/15 second.

[0019]

When processing a write request from the NTSC encoder 42, the mediation circuit 30a outputs a predetermined start signal to the processing circuit 30b in response to a write request input. An SDRAM read circuit 34b, in turn, reads YUV data out of the SDRAM 38. Also, a buffer control circuit 32b writes the YUV data read by the SDRAM 38 onto the buffer 26b. The processing circuit 30b generates an end signal when 64-pixels YUV data have been read out, similarly to the above. This puts the buses 28 and 36 open. This operation is repeatedly done, whereby 1-frame low resolution YUV data is read out of the SDRAM 38 in 1/30 second. Incidentally, the buffer 26b is also configured by a dual port SRAM having a capacity to store 128 pixels of YUV data.

[0020]

The SDRAM 38 includes a bank A and bank B, as shown in Figure 3. A bank switch circuit 40 outputs a bank switch pulse having a level varying every 1/15 second, based on vertical and horizontal synchronizing signals outputted from the SG 16. The SDRAM write circuit 34a assigns a write destination as a bank A when the bank switch pulse is in a high level, and as a bank B when the bank switch pulse is in a low level. On the other hand, the SDRAM reads circuit 34b assign a read destination as a bank B when the bank switch pulse is in a high level, and as a bank A when the bank switch pulse is in a low level. That is, the write and read operations to and from the SDRAM 38 are complementarily done wherein, when one bank is being written by data, the other bank is read of data.

[0021]

As described above, it takes 1/15 second to write 1 frame of YUV data whereas 1-frame YUV data is completely read out in 1/30 second. Also, the level of a bank switch

pulse is changed at an interval of 1/15 second. Due to this, while the YUV data of a current frame is written to one bank, the YUV data of the preceding frame is repeatedly read out twice. In this manner, there is difference between a time period required for writing and a time period required for reading. Accordingly, if there is provided only one bank, read scanning will outpace write scanning. This results in appearance of a horizontal line on the monitor 44. In order to eliminate such a problem, this embodiment provides the SDRAM 38 with two banks so that write and read operations to and from the banks can be made in a complementary manner.

[0022]

The buffer read circuit 42a provided in the NTSC encoder 42 reads YUV data stored in the buffer 26b at a quarter rate of a clock of writing. Furthermore, the read YUV data is encoded by an NTSC format. The encoded data is converted by a D/A converter 54 into an analog signal to be outputted onto the monitor 56. As a result, through-images are displayed on the monitor 56.

[0023]

In this manner, when outputting through-images, thinning out is performed on high resolution YUV data to be created every 1/15 second. Thus, YUV data with a decreased resolution down to as low as nearly VGA is outputted from the thinning-out circuit 24 every 1/15 second. That is, the number of pixels is decreased, the pitch of pixels is increased at thinned-out portions, and the data amount per unit time is decreased. The time period occupied over the buses 28 and 36 in transmission of a low resolution YUV data to the SDRAM 38 is reduced to a half of the conventional. In the conventional technique, since the resolution is lowered at a time of the output from the CCD imager 12, each frame of the low resolution YUV data has to be written to the SDRAM 38 at an interval of 30 seconds. Contrary to this, in this embodiment the occupation ratio over the

buses 28 and 36 can be reduced to a half of the conventional because the low resolution YUV data of each frame may be written within 1/15 second. That is, similar to the conventional technique, it is possible to reduce the occupation ratio in addition to prevention of process failure.

[0024]

However, the low resolution YUV data must be completely read out of the SDRAM 38 within 1/30 second. Accordingly, the occupation ratio over the buses 28 and 36 during reading is twice a ratio of writing. In other words, the reading from SDRAM 38 is at a twice rate of a rate of writing to the SDRAM 38. To realize this, the present embodiment provides two banks in the SDRAM 38 so that the bank to be written and the bank to be read are switched between in a complementary manner. Thus, the through-image displayed on the monitor 44 is prevented from being deteriorated in image quality.

[0025]

If the operator operates the shutter button 54, the CPU 46 connects the switch SW1 to the signal processing circuit 22. Also, the gate signal to the AND circuit 42c shown in Figure 2 is decreased to a low level to apply gating to a write request. This disables the thinning-out circuit 24, the SDRAM read circuit 34b and the buffer control circuit 32c. The high resolution YUV data outputted from the signal processing circuit 22 is written to the buffer 26a without being processed of thinning-out. The high resolution YUV data is greater in the number of pixels than the low resolution YUV data, hence requiring a correspondingly longer time in being written onto the SDRAM 38. However, the occupation ratio over buses 28 and 36 is decreased correspondingly to suspension of data reading from the SDRAM 38. This reduction of occupation ratio is allocated to data writing onto the SDRAM 38. Consequently, there is no possibility that process failure

occurs during writing the high resolution YUV data onto the SDRAM 38.

[0026]

When the high resolution YUV data has been completely written to the SDRAM 38, i.e., when elapsing 1/15 second from depressing the shutter button 54, the CPU 46 also reduces to a low level the gate signal to be supplied to the AND circuit 22c shown in Figure 2. This applies gating also to the read request, thus suspending the writing to the SDRAM 38.

[0027]

Incidentally, the switch SW2 is connected to a black image generating circuit 41 in response to operation of the shutter button 54. This supplies black image data to the NTSC encoder 42. Thus, a black image is displayed on the monitor 44 simultaneously with pressing on the shutter.

The 1-frame high resolution YUV data stored within the SDRAM 38 is delivered to the JPEG CODEC 45 via the buffer 26c where it is subjected to JPEG compression. The resulting compression data is once written to the SDRAM 38, and thereafter recorded onto a memory card 50. After completing the recording, the switch SW2 is returned and further the gate signal to be supplied to the AND circuit 42c is returned to the high level. Due to this, the high resolution YUV data stored within the SDRAM 38 is read out, and the display on the monitor 44 is turned from the black image to a freeze image. When the freeze image is displayed, the SDRAM 38 is kept suspended from being written on, providing a corresponding amount of vacancy to the buses 28 and 36. Accordingly, no process failure will occur in the buffer 26 despite the number of pixels of the high resolution YUV data is greater than that of the low resolution YUV data.

[0028]

Incidentally, the monitor 44 has a resolution that is lower than any of the high

resolution YUV data and the low resolution YUV data. Consequently, the NTSC encoder 42 performs thinning-out on the high resolution YUV data and low resolution YUV data in conformity to their number of pixels.

The CPU 46 processes concretely a flowchart shown in Figure 4 and Figure 5. First, in step S1 DMA is started for a camera signal process block. That is, the SG 15 is started, and the switch SW1 is connected to the thinning-out circuit 24 and a high level gate signal is supplied to the signal processing circuit 22. The signal processing circuit 22 writes low resolution YUV data onto the buffer 28 and sends a read request to the memory control circuit 30. As a result, the low resolution YUV data is written to the SDRAM 38. Then, the CPU 46 in step S3 starts DMA for an encode block. That is, a high level gate signal is delivered to the NTSC encoder 42. Due to this, a write request is sent to the memory control circuit 30, and the low resolution YUV data read out of the SDRAM 34 is written to the buffer 26b. The NTSC encoder 50 further processes the low resolution YUV data written on the buffer 26b. As a result, through-images are displayed on the monitor 44.

[0029]

If the shutter button 88 is operated by the operator, the CPU 46 in step S5 determines "YES". Then, in step S7 the switches SW1 and SW2 are respectively connected to the signal processing circuit 22 and the black image generating circuit 41. In step S9 a gate signal to be supplied to the NTSC encoder 42 is reduced to a low level. Accordingly, the high resolution YUV data is written to the SDRAM 38 whereby a black image is displayed on the monitor 44. In step S11 it is determined whether 1/15 second has been elapsed from depressing the shutter button 54 or not. If "YES", then in step S13 a gate signal to be supplied to the signal processing circuit 22 is lowered from a high level to a low level. Due to this, the writing to the SDRAM 38 is suspended.

[0030]

Subsequently, in step S15 the high resolution YUV data is recorded. If the recording process has been completed, then in step S17 "YES" is determined. In respective steps of S19 and S21, the switch SW2 is returned and the gate signal to be supplied to the NTSC encoder 42 is returned to the high level. Accordingly, a freeze image is displayed in place of the black image on the monitor 44. In step S23 it is determined whether a predetermined time has elapsed from the operation of the shutter button 54 or not. If "YES", then in step S25 the switch SW1 is returned. In step S27 the gate signal to be supplied to the signal processing circuit 22 is returned in level. Then the process returns to the step S5. As a result, through-images are displayed again on the monitor 44.

[Brief description of the drawings]

[Figure 1]

Figure 1 is a block diagram showing one embodiment of the present invention;

[Figure 2]

Figure 2 is a block diagram showing one part of the Figure 1 embodiment;

[Figure 3]

Figure 3 is an illustrative view showing one SDRAM;

[Figure 4]

Figure 4 is a flowchart showing one part of operation in the Figure 1 embodiment;

and

[Figure 5]

Figure 5 is a flowchart showing another part of operation of the Figure 1 embodiment.

[Explanation of reference characters]

10 ... digital camera
22 ... signal processing circuit
24 ... thinning-out circuit
28, 36 ... bus
30 ... memory control circuit
38 ... SDRAM
42 ... NTSC encoder

[Document name] ABSTRACT

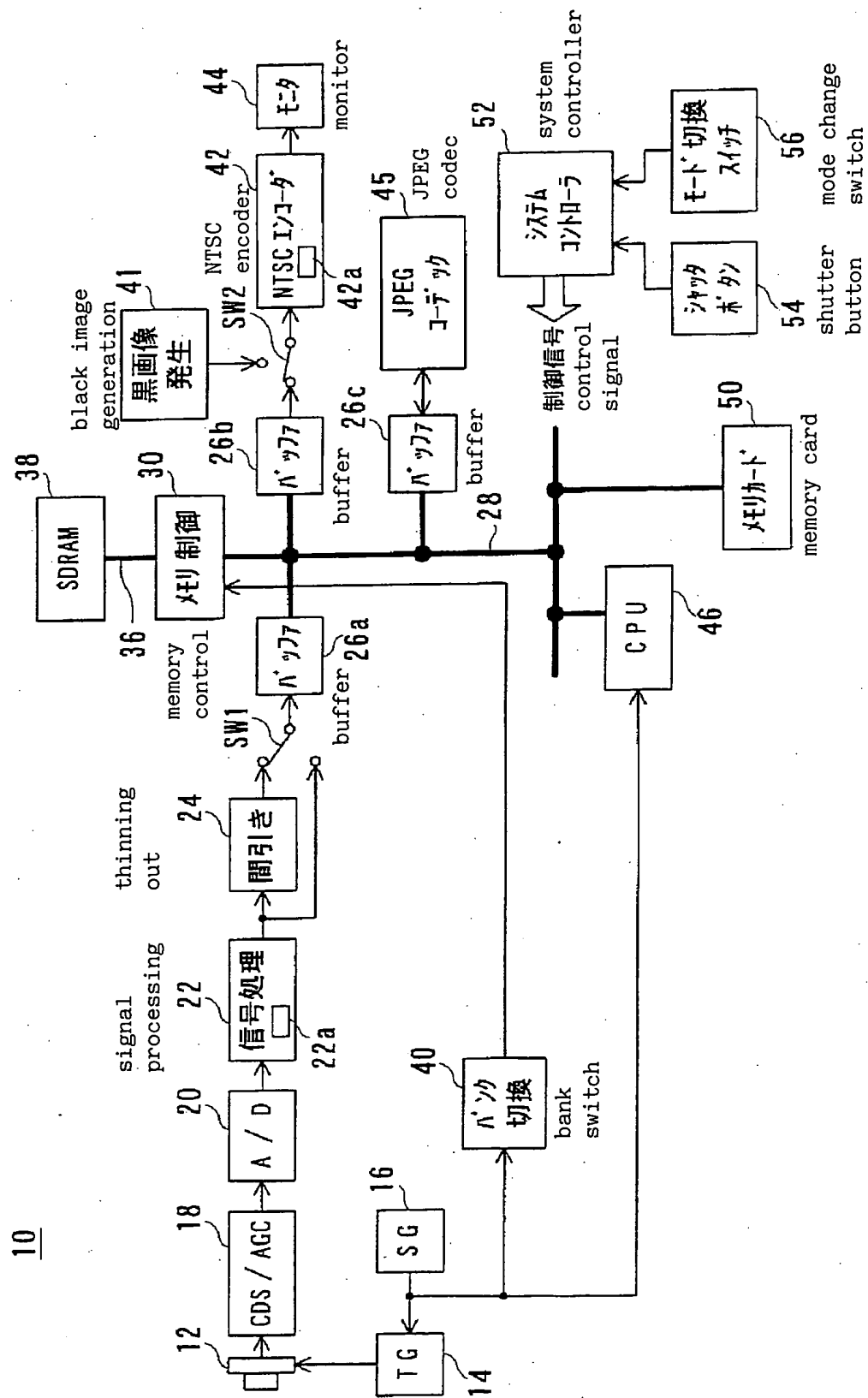
[Abstract]

[Structure] When outputting through-images on the monitor 44, high-resolution YUV data outputted from a signal processing circuit is thinned out and created into low-resolution YUV data. The low resolution YUV data of a current frame is written to one of banks formed within an SDRAM in 1/15 second. On the other hand, the low resolution YUV data of the preceding frame is read out of the other bank in 1/30 second. That is, reading is made twice within 1/15 second. The low resolution YUV data thus read is thereafter processed by an NTSC encoder and outputted onto the monitor 44.

[Effect] Due to reduction in data amount, no processing failure occurs. In addition, since a write operation and a read operation are performed on banks different from each other, the operation on one area will not outpace the operation on the other area. Thus, outputted images are free from disturbance.

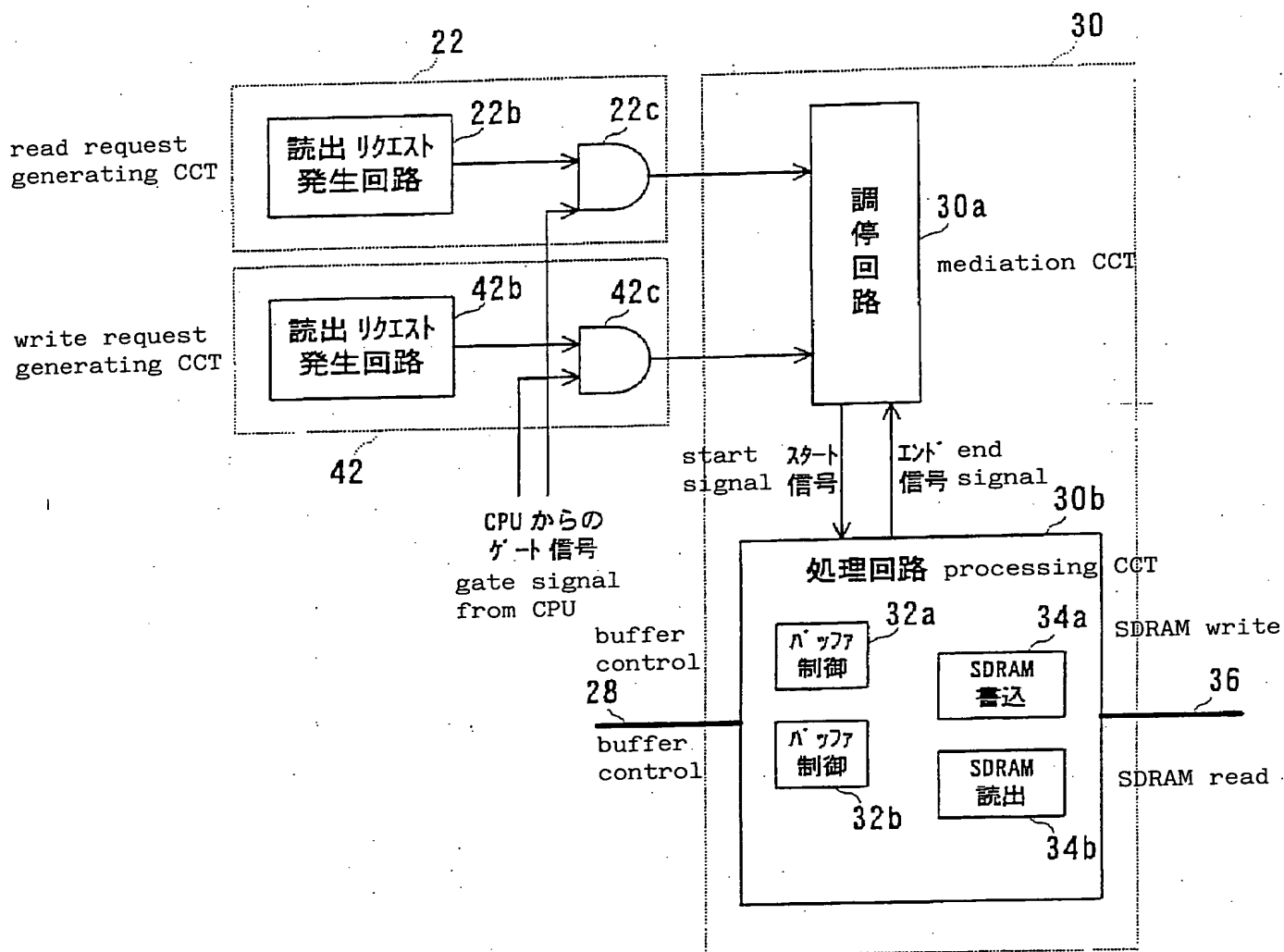
[Selected figure] Figure 1

【図 1】 Figure 1





【図 2】 Figure 2

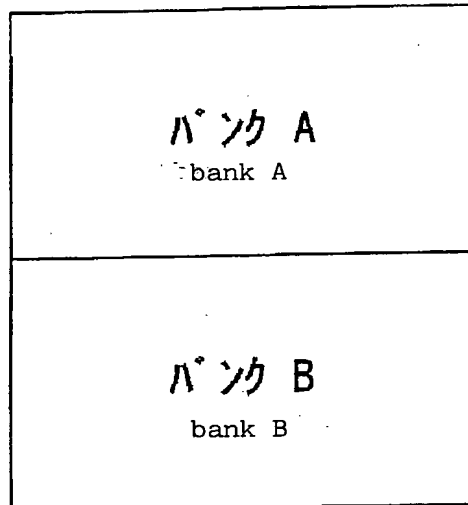




【図 3】

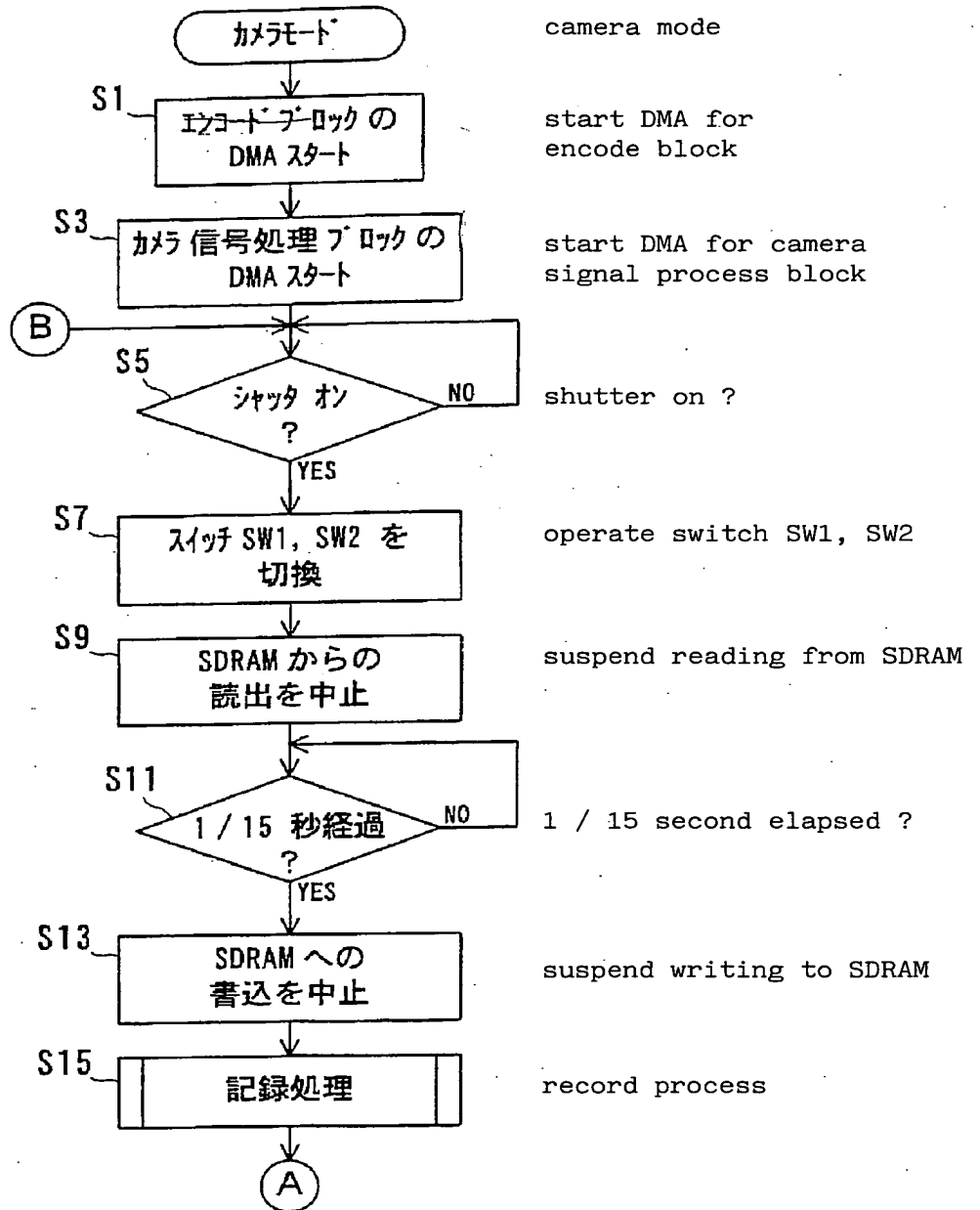
Figure 3

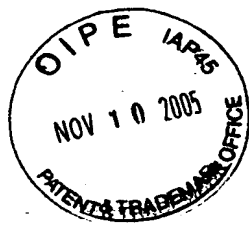
38





【図4】 Figure 4





【図 5】 Figure 5

